독립채널에 비해 8배의 클럭 속도를 높이는 테스트 방법 구현
Clock Speed up to Eight Times Faster than the Single Channel

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***Abstract*—Since each channel can run maximum speed of 200MHz in the FLEX, Teradyne Automatic Test Equipment (ATE), multiplexing 8 digital channels can create a signal with a data rate up to eight times faster than the single channel. And only limited factor is the pulse width of Pin Electronics which cause the speed drop.**

I. Introduction

Since each channel can run maximum speed of 200MHz in the FLEX, Teradyne Automatic Test Equipment (ATE), multiplexing digital channels can create a signal with a data rate up to eight times faster than the single channel. This method combines up to 8 HSD (High Speed Digital) channels to achieve the clock speed of up to 1.6GHz, 200MHz × 8HSD channels. This capability is called the High Frequency Multiplex (HFMUX).

The following figure1 shows the FLEX of which channel can run maximum speed of 200MHz.

Fig.1 Teradyne, FLEX

HFMUX connects any combination of up to eight digital channels on two adjacent timing generators through OR gates to one or two output channels.

And also, HFMUX can source a high speed data stream and can be programmed with pattern data. HFMUX mode generates a data stream by programming both the edge location and data for each selected channel individually. The ORed output from the selected channels is delivered to the DUT. This mode differs from conventional multiplex mode. In conventional multiplex mode, digital channels can drive and receive. In HFMUX mode, however, receive and HiZ formats are not available. HFMUX is drive only [1].

Because of the faster scan speed and depth with the eight channels, HFMUX can be used for scan data.

This paper introduces technical background of multiplexing 8 HSD channels to get the speed up to 1.6GHz. And it also introduces how to get a frequency of more than 200MHz with considerable points.

II. Technical Background

The FLEX digital instrument offers expanded capability (MTO, Scan, DSSC, and Differential Pin) integrated with 48 digital channels on a single instrument board. The data rate enabling of the HSD200 instrument (50 MHz, 100 MHz and 200 MHz) allows the user to adjust the performance and cost of their system based on their device testing needs.

The figure2 shows the typical HSD200 digital board.

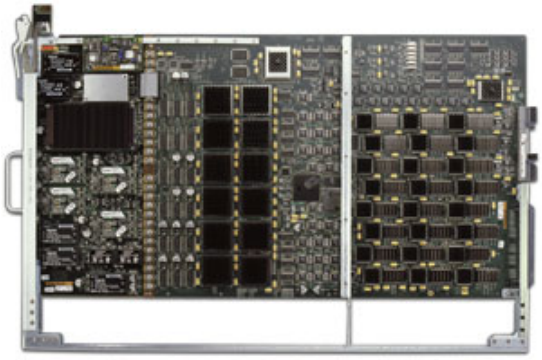

Fig.2 HSD200 Digital Board

Each digital channel card contains two groups of eight channels that can be multiplexed.

The first group of the digital channel card consists of channels from 13 to 16 and channels from 21 to 24. And the second group of the digital channel card consists of channels from 29 to 32 and channels from 37 to 40.

Connect one eight-channel group as a Multiplex channel while the other eight-channel group can make up another channel. Multiplexing the channels in any combination is possible. The only restriction is that channel 13 must be one

of the multiplexed channels in the first group and the channel 29 must be one of the multiplexed channels in the second group since the outputs depends on these channels. However channels between these two groups cannot be mixed. And channels excepted from multiplexing can be used for any other purpose.

The figure3 shows an example of typical HFMUX channels on a digital channel card.

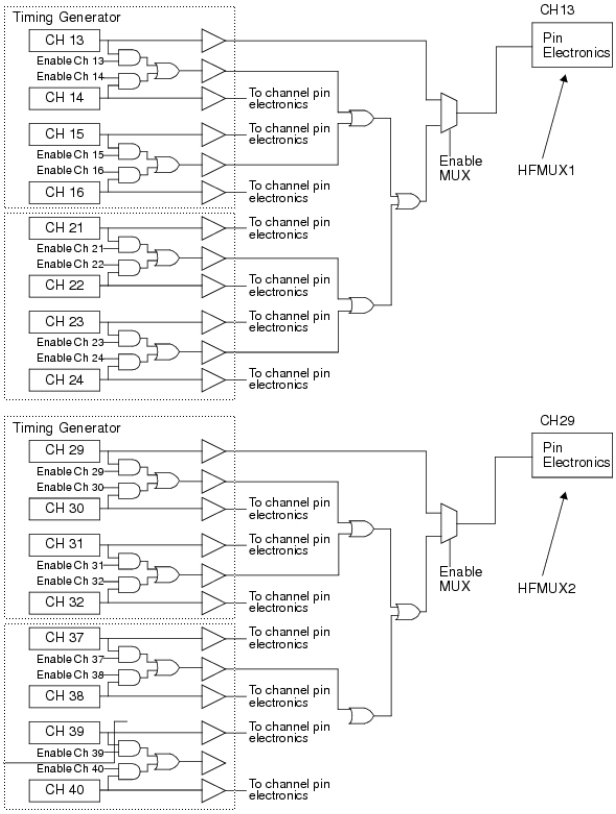

Fig.3 Typical configuration of HFMUX channels on a digital channel

And the figure4 shows an example of HFMUX signal output of the first group and the second group.

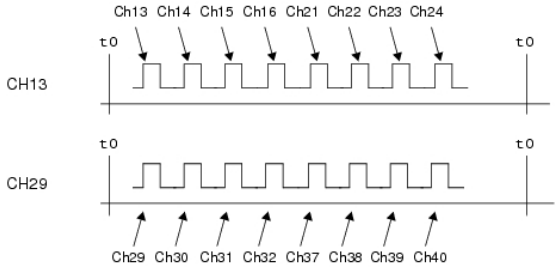

Fig.4 Output signals for typical channels on a digital channel

The figure5 shows another possible configuration with eight channels multiplexed by two channels. The multiplexed signals are delivered to the DUT on the pin electronics of two digital channels within the eight-channel group (labeled CH13 and CH21 in the figure4).

Pairs of channels are enabled and ORed together inside the timing generator. On the digital channel card, two additional OR gates combine the pairs and a final OR gate combines the channels. The combined signal is delivered to the pin electronics of the lowest numbered channel of the two timing generators. A multiplexer selects the combined signal or normal I/O signal.

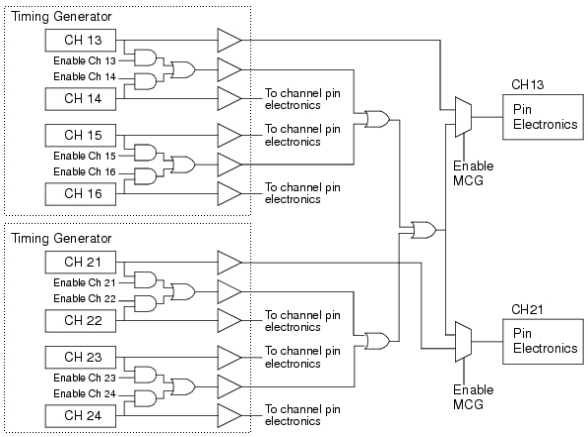

Fig.5 HFMUX with eight channels multiplexed to two channels

Only the upper output channel, labeled CH13 in the figure5, can be completely calibrated since both channels CH13 and CH21 receive timing signals from the other channels. Any timing errors in the lower channel (CH21) might be caused by the DIB path lengths (or the trace) and pin electronics.

III. Programming Procedure

To get a frequency of more than 200MHz, follow this procedure to create a test program using high-frequency multiplex (HFMUX).

Enter the pins on a Pin Map sheet. The pins must be Input type.

The figure6 shows two channels, channel 13 and 14 that will be muxed in a Pin Map sheet. These pins will be used for the first HFMUX channel on the digital channel card.

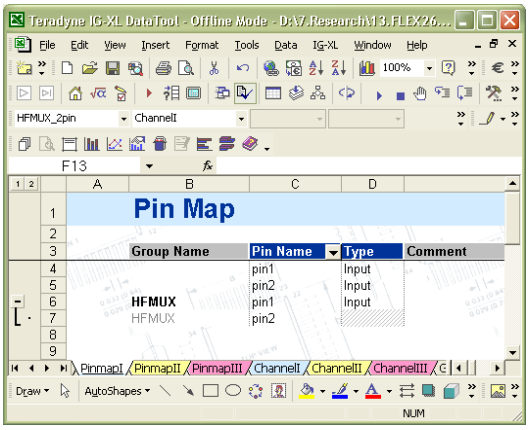

Fig.6 HFMUX Pin Map

On a Channel Map sheet, map the pins to some or all of the 16 standard digital channels that make up the two HFMUX channels. Also the pins must be Input type. One of the pins must be mapped to either digital channel 13 or 29.

The figure7 shows channel 13 and 14 mapped to pin name pin1 and pin2 for the first HFMUX channel.

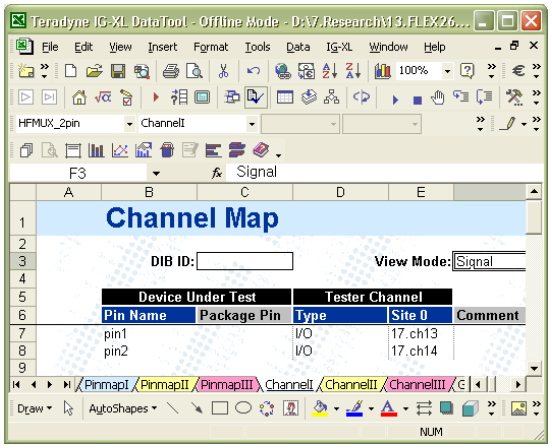

Fig.7 Mapping Pins to Digital Channels for HFMUX

Define values for input voltages and current loads to be applied to the DUT. The figure8 shows 3V Voltage in High (Vih) on pin levels sheet. Vih on pin levels sheet can be applied from -1V to 6V.

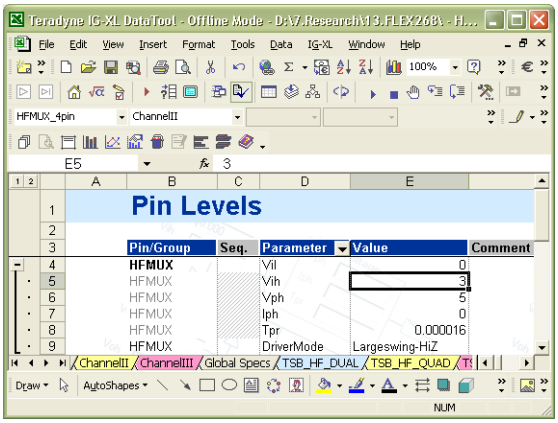

Fig.8 HFMUX Pin Levels

Also with Pin Levels sheet, specify the pins on a Time Sets (Basic) sheet with HFMUX mode in the Pin/Group Setup field, as shown in the figure9.

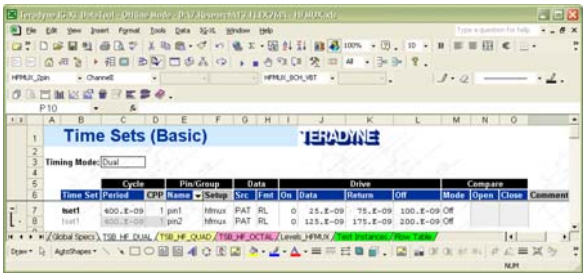

Fig.9 Timing set for the HFMUX

The specified pins must have been previously mapped to channels that make up an HFMUX channel. Two pins must be specified for each HFMUX channel and one of the pins must be mapped to either channel 13 or 29. Also specify the Drive Data and Drive Return and the Data Src and Data Fmt for each pin so the desired data stream is delivered from the HFMUX channel.

On the obstacles with rising time, falling time, and the minimum pulse width in timing mode this paper will discuss later in the results of HFMUX pulse section.

After time set setting is finished, include each pin in the pattern file with data that is appropriate to achieve the desired data stream. The following figure10 shows that binary formatted pattern for HFMUX (*.pat). And the following figure11 shows that ASCII formatted pattern for HFMUX (*.atp).

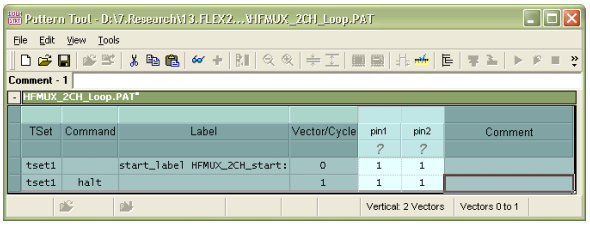

Fig.10 Binary formatted pattern

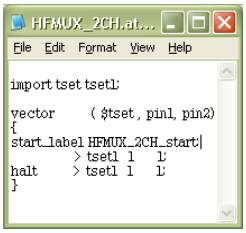

Fig.11 ASCII formatted pattern

Finally, define the order in which tests are executed. There are two choices to define the test. The first method is using template. The following figure12 shows 2channel HFMUX using Functional template.

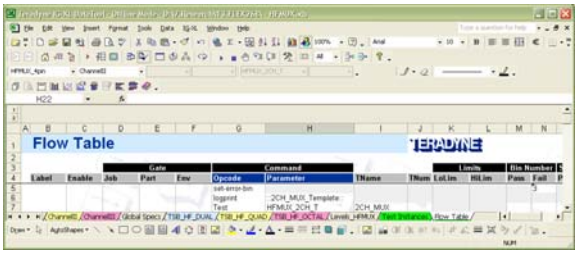

Fig.12 Flow Table for the HFMUX

And also define the tests that will be applied to the DUT and enter the parameters for each test instance.

The other way to define the test is coding by the VBT (Visual Basic for Test), not by functional template, as shown in the figure13.

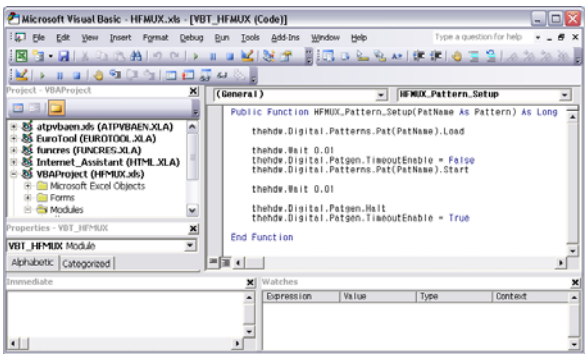

Fig.13 VBT code for the HFMUX pattern load and start

IV. Results of HFMUX Pulse

IG-XL™ validation checks whether the specified pins are mapped to channels that make up an HFMUX. And two pins will be used in this case. Also one of the pins will be mapped to either channel 13 or 29.

Drive off, D3 in IG-XL™, should come before Drive data, D1, of the next channel. Also edges should be programmed for each channel used in multiplexing.

Multiplexing channel 13 and channel 14 in HFMUX with channel 13 result output are shown in the figure14.

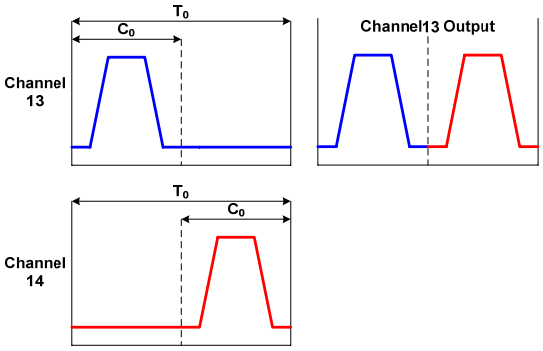

Fig.14 Multiplexing Ch13 & Ch14 with Ch13 output

Since the combined output of the specified channels is ORed, choose the Return to Low (RL) format in the field of Data Src and Data Fmt such that the state of any channel after driving is not high.

From the IG-XL™ debug display with high-frequency multiplex (HFMUX) programming procedure shows waveform in Horizontal mode, HRAM data can be in Symbolic or Waveform mode. These display modes are available in both Pattern Tool HRAM Overlay mode and in HRAM Pattern Tool.

The figure15 shows HRAM display of 2channel HFMUX in Waveform mode. It is exactly same as previous figure 14, concept of multiplexing 2channels.

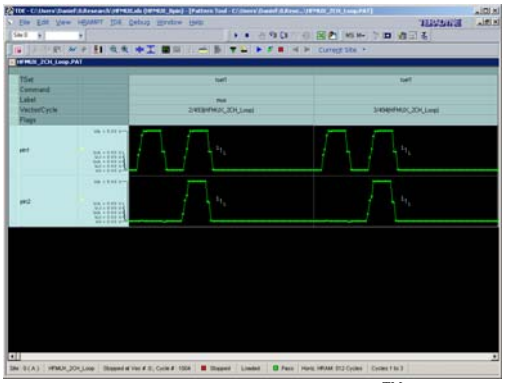

Fig.15 HRAM display of 2channel from IG-XL™ debug display

The following table1 shows the specification of oscilloscope used for the HFMUX measure [2].

Model	Band width	Sample Rate	Record Length
TDS3032B	300MHz	2.5 GS/s	10 K sample

Table.1 Oscilloscope Specification

The figure16 shows capture from oscilloscope, Tektronics TDB3032B, display of 2channel HFMUX.

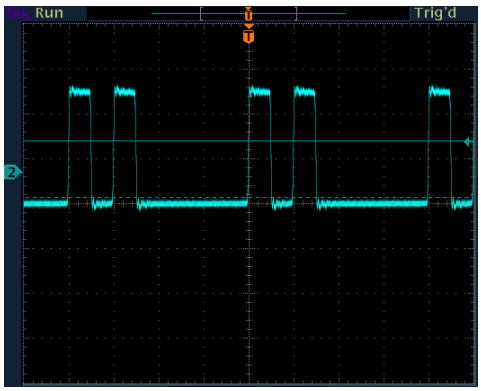

Fig.16 Oscilloscope display of 2channel multiplex

From HRAM pattern tool, HSD200 can multiplex up to 8 channels, theoretically. The following figure17 shows HRAM display of 4channels and the following figure18 shows 8 channels HFMUX in waveform mode.

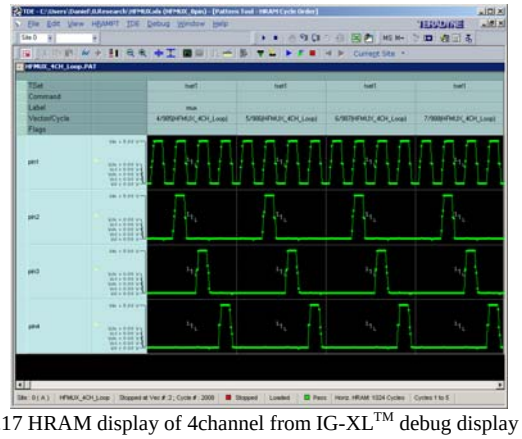

Fig.17 HRAM display of 4channel from IG-XL™ debug display

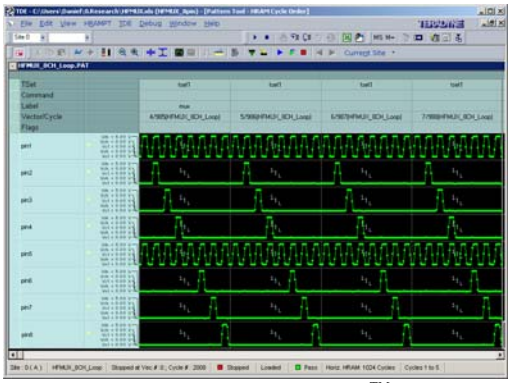

Fig.18 HRAM display of 8channel from IG-XL™ debug display

The real obstacle here is the front end driver of an HSD channel called Pin Electronic (PE). Even if best designed PE, which has very low rise and fall time can reduce the theoretical speed of 1.6GHz (200MHz × 8HSD channels). However it is still usable impressive speed of 400MHz just by multiplexing only 2 channels. Discuss more about voltage in high level compare to output of digital channel, minimum pulse width of PE is limiting factor [3].

The following figure19 shows channel block diagram of Pin Electronics (PE).

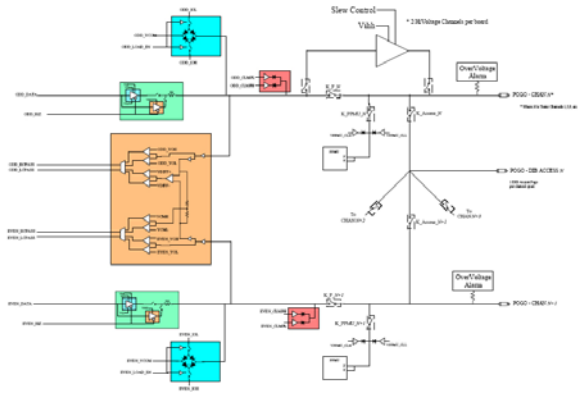

Fig.19 Channel block diagram of Pin Electronics

Already mentioned above, the real obstacle here is the front end driver of an HSD channel called Pin Electronic (PE). And the concepts of the minimum pulse width and the maximum rise time and fall time at different Vih level are shown in figure20.

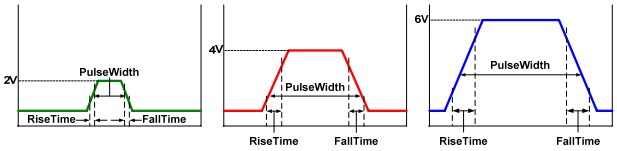

Fig.20 Min. pulse width and max. rise and fall time at different Vih level

The figure21 shows that both rising and falling time measurement in the FLEX are shown. Normally 20% to 80% of rising and falling time is the captured point.

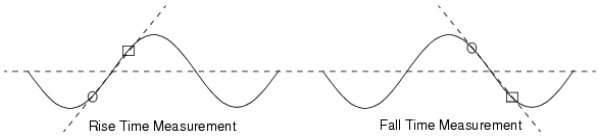

Fig.21 Rise and fall time measurement example

Many experimentation shows that rising and falling time are depend on the voltage in low, Vil, and the voltage in high, Vih. Table2 shows that maximum rising and falling time are captured from the oscilloscope.

Measure	2V Vih	4V Vih	6V Vih
Rise/Fall time	0.7~1.1ns	1.5~1.8ns	2~2.3ns

Table.2 Rise and fall time capture from the oscilloscope

The following figure22 shows the pulse width measurement in FLEX.

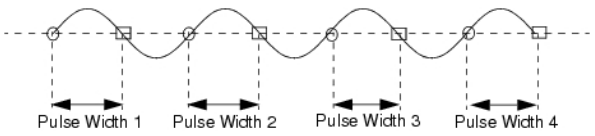

Fig.22 Example of Pulse width measurement

The following table3 shows the pulse width also related on the Vil and Vih.

Measure	2V Vih	4V Vih	6V Vih
Pulse width	1.8~2ns	2.2~2.5ns	2.8~3ns

Table.3 Pulse width capture from the oscilloscope

Rise and fall time and Pulse Width are increased in proportion to the applied voltage of VIL/VIH (-1V~-6V). The following figure23 on the left shows that 1V Vih output of HFMUX channel 13 capture from the oscilloscope. And the following figure23 on the right shows that 5V Vih output of channel 13.

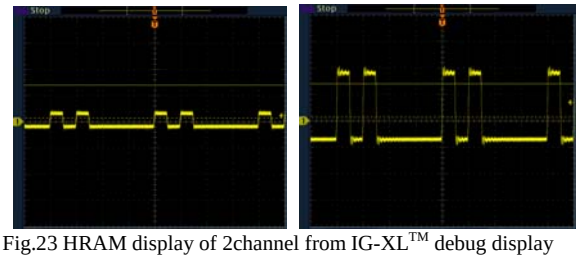

Fig.23 HRAM display of 2channel from IG-XL™ debug display

V. Conclusion

In this paper, we introduce technical background of multiplexing 8 HSD channels to get the speed of up to 1.6GHz. And also introduces how to get a frequency of more than 200MHz, with considerable points.

Any wiring on the device interface board is unnecessary. HFMUX connects any combination of up to eight digital channels on two adjacent timing generators through OR gates to one or two output channels internally. The ORed output from the selected channels is delivered to the DUT.

Output must be channel 13 (one output) or channel 13 and 21 (two outputs) for the first group. Output must be channel 29 (one output) or channel 29 and 37 (two outputs) for the other group.

All channels multiplexed must be Drive format only. Also receive and HiZ formats are not allowed.

Any combination of channels within the same group can be used as High Frequency Drivers. And any channels that are not used in multiplexing can be used for other usage, such as normal Drive and Receive formats (I/O).

Customer, who has 100MHz - HSD200 license rather than 200MHz, can generate 200MHz clock by multiplexing only two channels.

Normally with 200MHz - HSD200 license, by multiplexing 8channels, maximum clock speed up to 1.6GHz can be achieved.

VI. References

[1] "IG-XL™ Help", Teradyne IG-XL 5.10.30

[2] "Tektronics TDS3032B Help", http://www.tektornics.com.

[3] "Beyond 200MHz: How to achieve it and what are the obstacles", TUG2004, May.2004.